PATENT APPLICATION
Doc. No. 8371-129
Client Ref. No. SLA0571

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Apostolos VOUTSAS and Yukihiko NAKATA		
Serial No.	09/945,063	Examiner:	George R. Fourson III
Filed:	August 31, 2001	Art Unit:	2823
For:	METHOD OF FORMING MULTI-LAYERS FOR A THIN FILM TRANSISTOR (TFT) AND THE DEVICE FORMED THEREBY		
Confirmation No.:	3014		

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT

Responsive to a communication, dated November 17, 2004, please amend the application as follows.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 7 of this paper.

PATENT APPLICATION
Attorney's Do. No. 8371-129
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TRANSMITTAL LETTER

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Responsive to the communication dated November 17, 2004, enclosed is an amendment in the above-identified application.

The fee has been calculated as shown below.

CLAIMS AS AMENDED					
For:	Number After Amendment	Previous Number	Extra	Rate	Additional Fee
Total Claims	19	19*	0	0x $9 =	$0
Independent Claims	2	2**	0	0x $43 =	$0
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT					$0

*greater of twenty (20) or number for which fee has been paid
**greater of three (3) or number for which fee has been paid

Enclosed for filing in the above-referenced application are the following:

☒ Notice of Limited Recognition Under 37 CFR § 10.9(b).
☒ Any deficiency or overpayment should be charged or credited to deposit account number 13-1703.

Customer No. 20575

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.

Hosoon Lee
Limited Recognition Under 37 CFR § 10.9(b)

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Signature
Natasha French

IN THE CLAIMS

1. (Previously Presented) A method of forming multi-layers for manufacturing a thin

film transistor (TFT) using multiple process chambers, comprising:

forming a first layer of silicon dioxide for the thin film transistor on a glass substrate using a first non-chemical physical vapor deposition in a first process chamber;

transferring the substrate including the first layer to a second process chamber without breaking vacuum;

sequentially forming a second layer of amorphous silicon for the thin film transistor in the second process chamber using a second non-chemical physical vapor deposition on the first layer without breaking vacuum for fabricating the thin film transistor; and

forming additional layers on top of the second layer for completing formation of the thin film transistor.

2. (Previously Presented) The method of claim 1, wherein the physical vapor deposition for forming the first layer and the second layer comprises pulsed-DC or RF sputtering.

3. (Currently Amended) The method of claim 1, wherein the first layer is formed using a gas mixture of Ar+$O2_2$ using a $SiO2_2$ target P-doped with a resistivity of 1-50 Ohms-centimeters.

4. (Currently Amended) The method of claim 3, wherein the first layer, the second layer and the additional layers form the thin film transistor into a liquid crystal ~~diode~~ display(LCD).

5. (cancelled)

6. (cancelled)

7. (cancelled)

8. (cancelled)

9. (cancelled)

10. (cancelled)

11. (cancelled)

12. (cancelled)

13. (cancelled)

14. (Original) The method of claim 1, wherein said forming a first layer is performed by sputtering using a first target comprising silicon dioxide.

15. (Original) The method of claim 1, wherein said forming a second layer is performed by sputtering using a target formed of a material selected from the group consisting of single crystalline silicon and polycrystalline silicon.

16. (Original) The method of claim 1, wherein the physical vapor deposition for forming the second layer comprises regular-DC, pulsed DC or RF sputtering.

17. (Withdrawn) A thin film transistor, comprising:

a transparent substrate;

a first layer formed on the substrate using a first physical vapor deposition; and

a second layer formed sequentially on the first layer using a second physical vapor deposition, without breaking vacuum.

18. (Withdrawn) The thin film transistor of claim 17, wherein the first layer is formed using pulsed-DC or RF sputtering.

19. (Withdrawn) The thin film transistor of claim 17, wherein the first layer is silicon dioxide.

20. (Withdrawn) The thin film transistor of claim 19, wherein the second layer is amorphous silicon.

21. (Withdrawn) A poly-Si thin film transistor, comprising:

a transparent substrate;

a first layer formed on the substrate using a physical vapor deposition; and

a second layer formed sequentially on the first layer, using the physical vapor deposition and an annealing process for crystallization, without breaking vacuum.

22. (Withdrawn) The thin film transistor of claim 21, wherein the physical vapor deposition for forming the first layer comprises pulsed-DC or RF sputtering.

23. (Withdrawn) The thin film transistor of claim 21, wherein the first layer is silicon dioxide.

24. (Withdrawn) The thin film transistor of claim 23, wherein the second layer is polycrystalline silicon.

25. (Withdrawn) A display device, comprising:

a transparent substrate;

a first layer formed on the substrate using a first physical vapor deposition; and

a second layer formed sequentially on the first layer using a second physical vapor deposition, without breaking vacuum.

26. (Withdrawn) The device of claim 25, wherein the first layer is formed using pulsed-DC or RF sputtering.

27. (Withdrawn) The device of claim 25, wherein the first layer is silicon dioxide.

28. (Withdrawn) The device of claim 27, wherein the second layer is amorphous silicon.

29. (Previously Presented) The method of claim 1, wherein no annealing is performed between forming a first layer and forming a second layer.

30. (Previously Presented) The method of claim 1 including using a mixture of He/Ar gas to form the second layer while introducing a hydrogen flow.

31. (Previously Presented) A method of forming multi-layers for manufacturing a thin film transistor (TFT) using multiple process chambers, comprising:

forming a first layer of silicon dioxide for the thin film transistor on a glass substrate using a first physical vapor deposition in a first process chamber;

transferring the substrate including the first layer to a second process chamber without breaking vacuum;

sequentially forming a second layer of amorphous silicon for the thin film transistor in the second process chamber using a second physical vapor deposition on the first layer without breaking vacuum for fabricating the thin film transistor; and

forming additional layers on top of the second layer for completing formation of the thin film transistor.

32. (Previously Presented) The method of claim 31, wherein forming the first layer is performed by sputtering using a first target comprising a silicon material selected from the group consisting of polysilicon and single-crystal silicon.

33. (Previously Presented) The method of claim 31, wherein the first layer is silicon dioxide and is sputter deposited from the first target with oxygen.

34. (Previously Presented) The method of claim 31, wherein the first layer is silicon dioxide and is sputter deposited from the first target with a reactive gas mixture comprising oxygen and He.

35. (Previously Presented) The method of claim 31, wherein the first layer is silicon dioxide and is sputter deposited from the first target with a reactive gas mixture comprising oxygen and H_2.

36. (Previously Presented) The method of claim 31, wherein the first layer is silicon dioxide and is sputter deposited from the first target with a reactive gas mixture comprising oxygen, He, and H_2.

37. (Previously Presented) The method of claim 31, wherein the first layer is silicon dioxide and is sputter deposited from the first target with a reactive gas mixture comprising oxygen and any one of Ar, Ne, or Kr.

38. (Previously Presented) The method of claim 31, wherein the first layer is silicon dioxide and is sputter deposited from the first target with a reactive gas mixture comprising oxygen, He, and any one of Ar, Ne, or Kr.

39. (Currently Amended) The method of claim ~~39~~ 38, wherein the reactive gas mixture comprises oxygen, He and Ar, and wherein a ratio of Ar in He is between approximately 3-20% Ar in Helium.

40. (Previously Presented) The method of claim 31, wherein the predetermined resistivity R1 is in a range of approximately 1-50 Ohm-cm.

REMARKS

Claims 1-4, 14-16 and 29-40 are pending.

Claims 5-13 have been cancelled.

Claims 17-28 stand withdrawn as non-elected and are hereby cancelled without prejudice for presentation in a divisional application.

Claims 1-4, 14-16 and 29-40 have been allowed.

Claims 35-40 were previously submitted as claims 36-41. They have been renumbered and are herewith submitted correctly under rule 126 as claims 35-40.

Claims 3, 4 and 39 have been amended to correct typographical errors as suggested by the Examiner.

No new matter has been added.

Applicant requests reconsideration and allowance of the claims in light of the above amendments and following remarks.

For the foregoing reasons, applicant believes that this application is in condition for allowance. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.

Hosoon Lee
Limited Recognition Under 37 § 10.9(b)

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Natasha French

BEFORE THE OFFICE OF ENROLLMENT AND DISCIPLINE
UNITED STATES PATENT AND TRADEMARK OFFICE

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Expires: July 16, 2005

Harry I. Moatz
Director of Enrollment and Discipline